

# MCR08BT1

Thyristor; logic level

Rev. 4 — 2 November 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Passivated, sensitive gate thyristor in a SOT223 plastic package.

### 1.2 Features and benefits

- Sensitive gate
- Surface mount package.

### 1.3 Applications

- General purpose switching and phase control
- Designed to be interfaced directly to microcontrollers, logic integrated circuits and low power gate trigger circuits.

### 1.4 Quick reference data

- $V_{DRM}, V_{RRM} \leq 200 \text{ V}$
- $I_{T(RMS)} \leq 0.8 \text{ A}$
- $I_{T(AV)} \leq 0.5 \text{ A}$
- $I_{TSM} \leq 9 \text{ A}$
- $I_{GT} = 50 \mu\text{A (typ)}$ .

## 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	cathode	<p>SOT223 (SC-73)</p>	<p>A — — — — K G sym037</p>
2	anode		
3	gate		
4	anode		

## 3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
MCR08BT1	SC-73	plastic surface mounted package with increased heat sink; 4 leads	SOT223



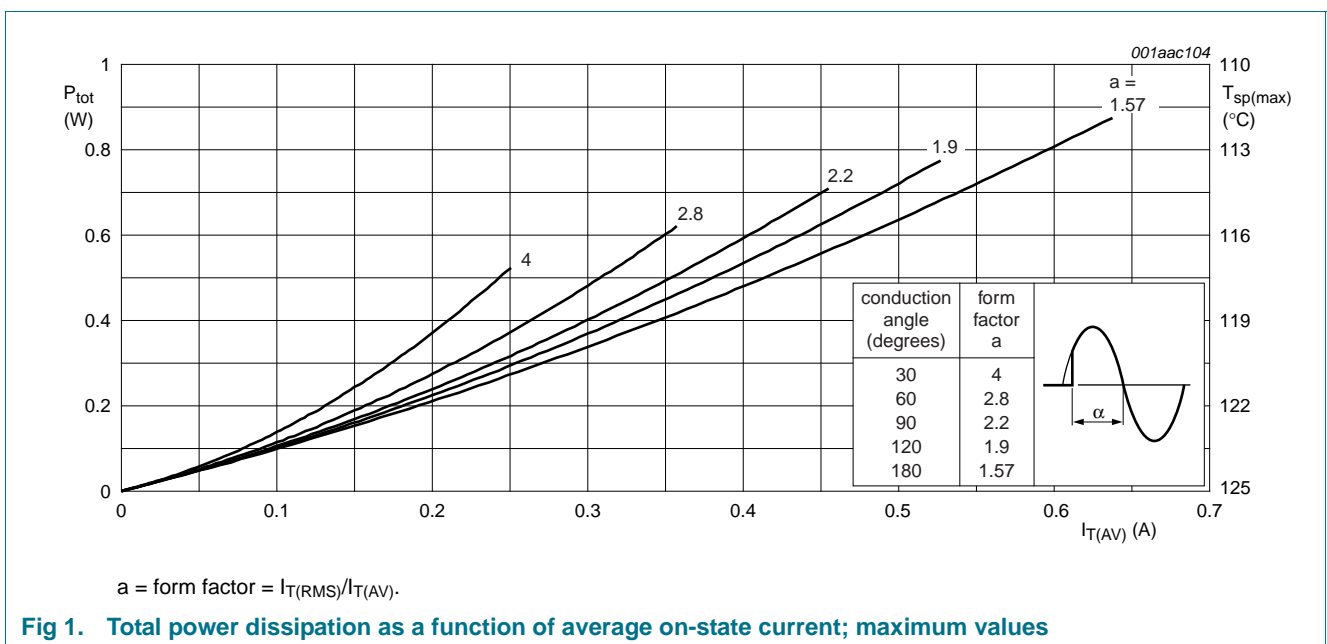
### 4. Limiting values

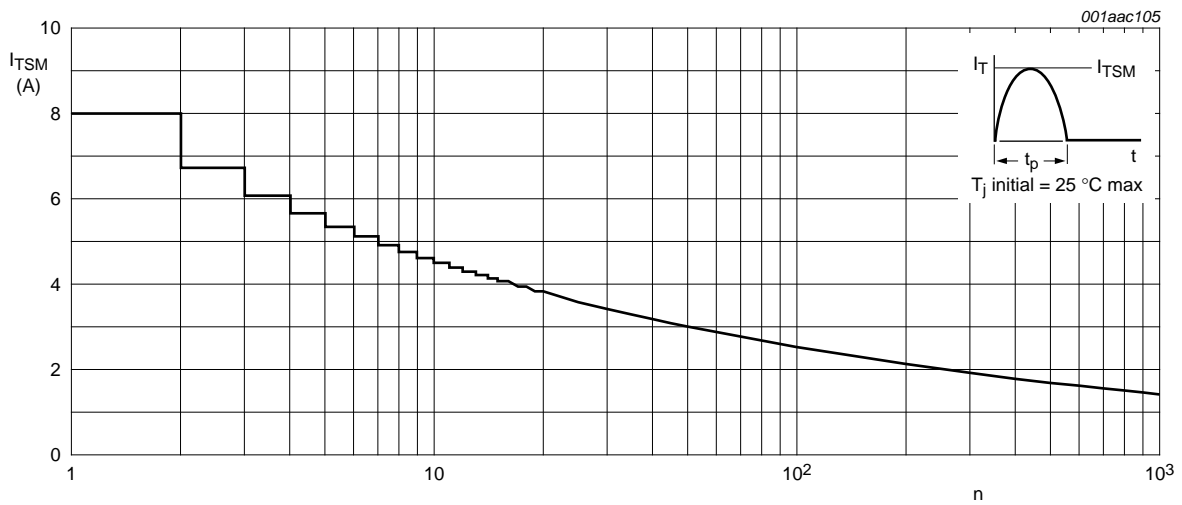
**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}, V_{RRM}$	repetitive peak off-state voltage		[1]	200	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112\text{ }^\circ\text{C}$ ; see <a href="#">Figure 1</a>	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see <a href="#">Figure 4</a> and <a href="#">5</a>	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ }^\circ\text{C}$ prior to surge; see <a href="#">Figure 2</a> and <a href="#">3</a>			
		$t = 10\text{ ms}$	-	8	A
		$t = 8.3\text{ ms}$	-	9	A
$I^2t$	$I^2t$ for fusing	$t = 10\text{ ms}$	-	0.32	$\text{A}^2\text{s}$
$dI_T/dt$	repetitive rate of rise of on-state current after triggering	$I_{TM} = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		-	1	A
$V_{GM}$	peak gate voltage		-	5	V
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	+150	$^\circ\text{C}$
$T_j$	junction temperature		-	125	$^\circ\text{C}$

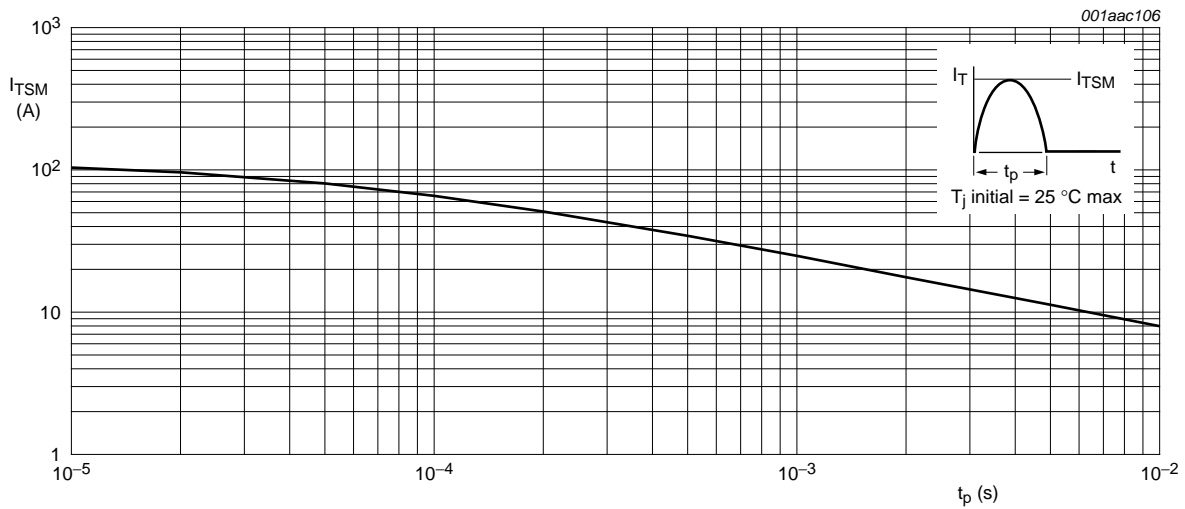
[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.





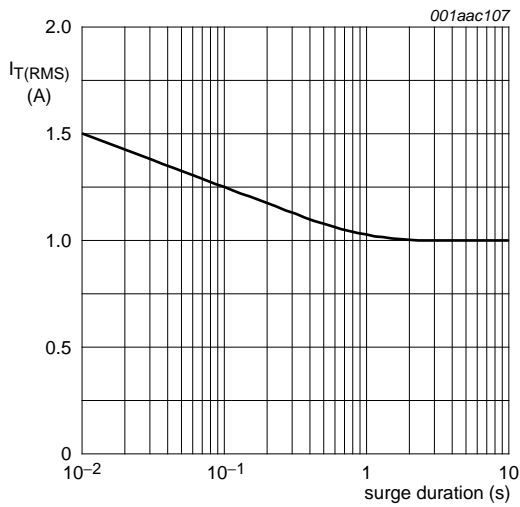
$f = 50$  Hz.

**Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**



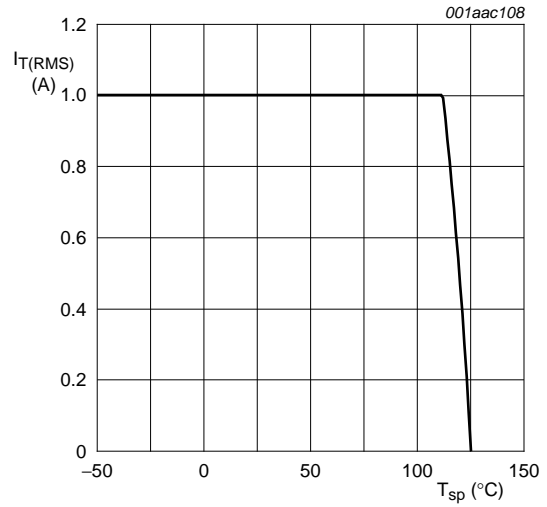
$t_p \leq 10$  ms.

**Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values**



$f = 50 \text{ Hz}; T_{sp} \leq 112 \text{ }^\circ\text{C}.$

**Fig 4.** RMS on-state current as a function of surge duration for sinusoidal currents; maximum values



$T_{sp} = 112 \text{ }^\circ\text{C}.$

**Fig 5.** RMS on-state current as a function of solder point temperature; maximum values

## 5. Thermal characteristics

**Table 4:** Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 6</a>	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted, minimum footprint	-	156	-	K/W
		printed-circuit board mounted, pad area as in <a href="#">Figure 14</a>	-	70	-	K/W

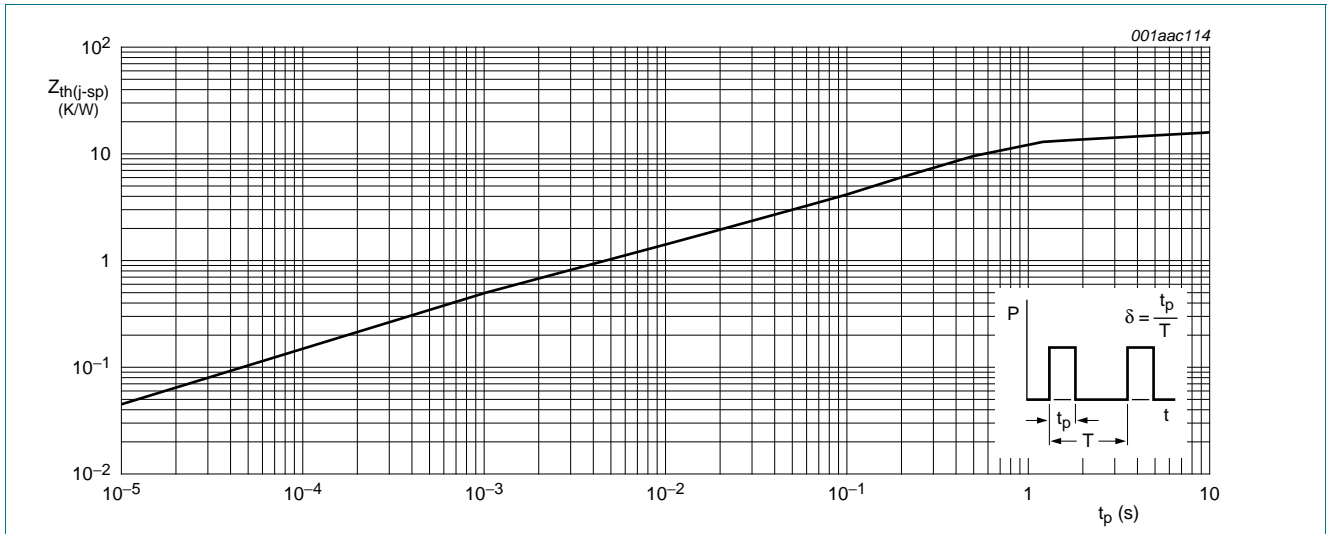


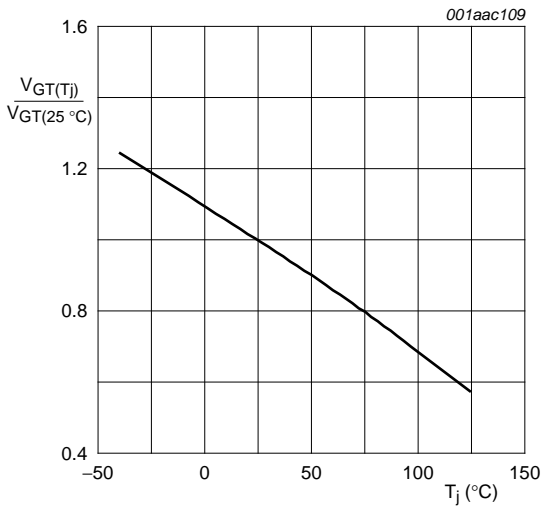
Fig 6. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

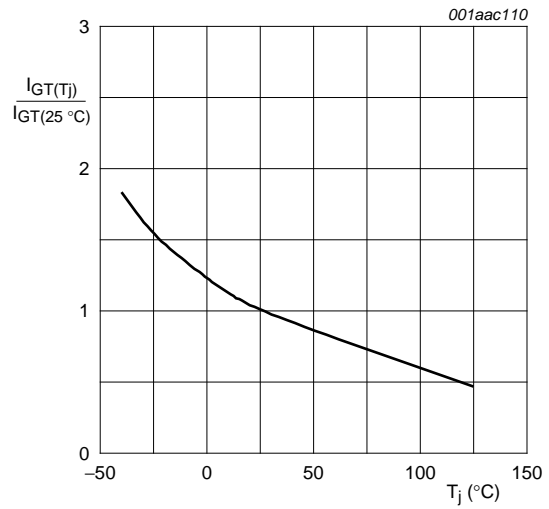
Table 5: Characteristics

$T_j = 25\text{ °C}$  unless otherwise specified.

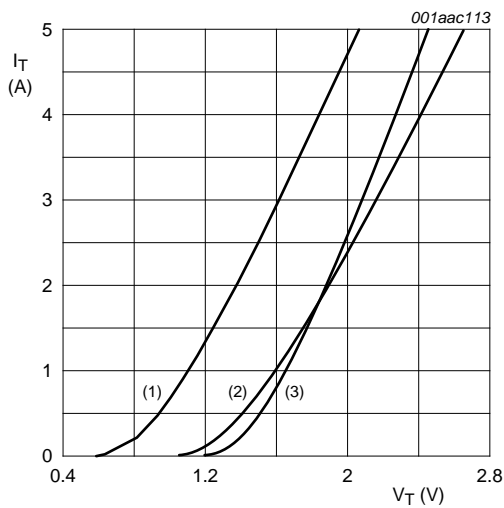
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; gate open circuit; see <a href="#">Figure 8</a>	-	50	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 10</a>	-	2	6	$\text{mA}$
$I_H$	holding current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 11</a>	-	2	5	$\text{mA}$
$V_T$	on-state voltage	$I_T = 1.2\text{ A}$ ; see <a href="#">Figure 9</a>	-	1.25	1.7	$\text{V}$
$V_{GT}$	gate trigger voltage	$I_T = 10\text{ mA}$ ; gate open circuit; see <a href="#">Figure 7</a>	-	0.5	0.8	$\text{V}$
		$V_D = 12\text{ V}$	-	0.5	0.8	$\text{V}$
		$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$	0.2	0.3	-	$\text{V}$
$I_D$	off-state leakage current	$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	$\text{mA}$
$I_R$	reverse current	$V_R = V_{RRM(max)}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	$\text{mA}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; exponential waveform				
		$R_{GK} = 1\text{ k}\Omega$	500	800	-	$\text{V}/\mu\text{s}$
		gate open circuit	-	25	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate controlled turn-on time	$I_{TM} = 2\text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$
$t_q$	circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; $I_{TM} = 1.6\text{ A}$ ; $V_R = 35\text{ V}$ ; $dI_{TM}/dt = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK} = 1\text{ k}\Omega$	-	100	-	$\mu\text{s}$



**Fig 7. Normalized gate trigger voltage as a function of junction temperature**

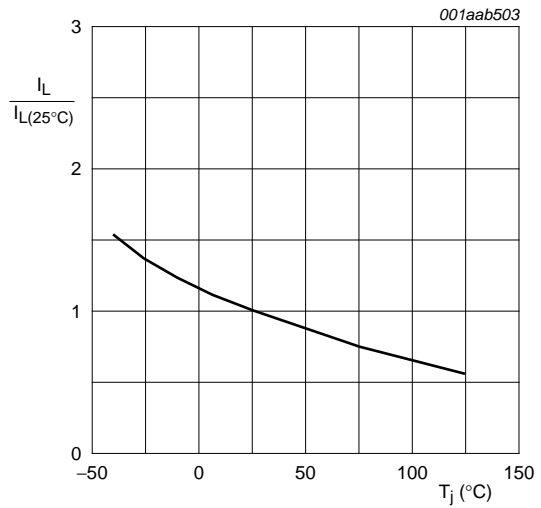


**Fig 8. Normalized gate trigger current as a function of junction temperature**



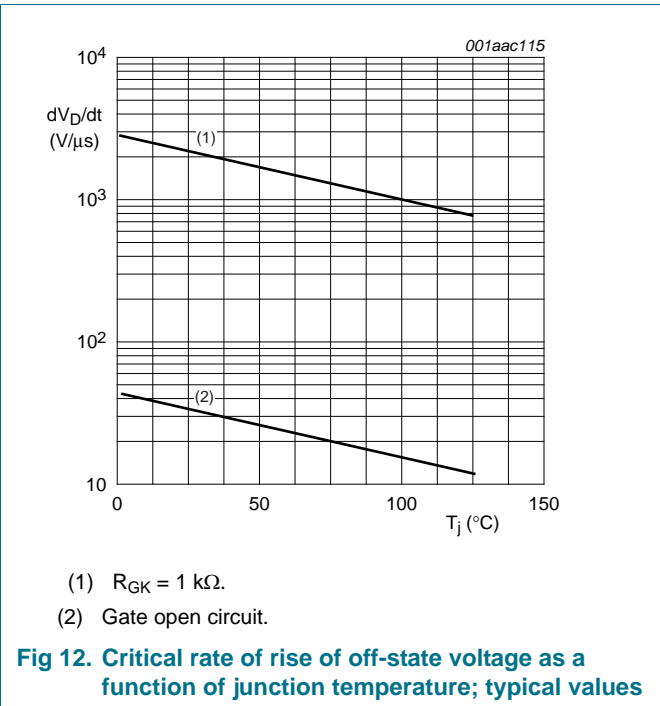
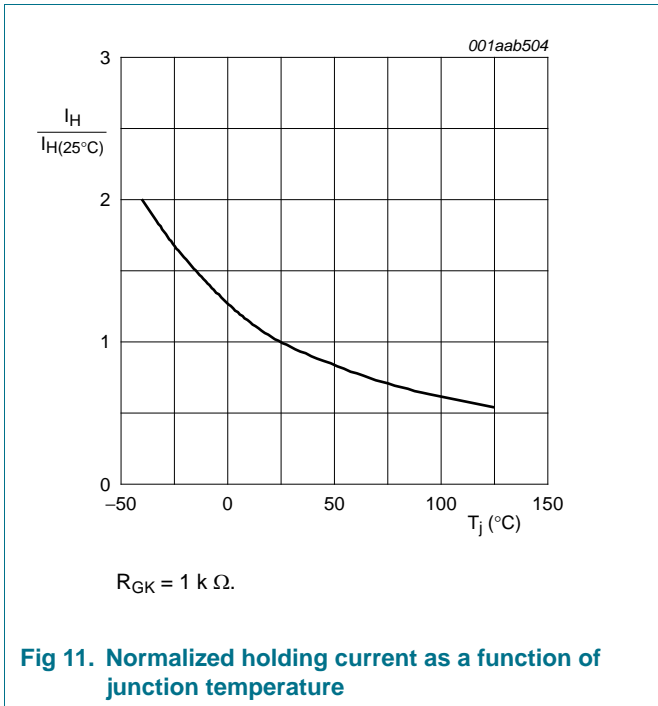
$V_O = 1.0 \text{ V.}$   
 $R_S = 0.27 \Omega.$   
 (1)  $T_j = 125 \text{ }^\circ\text{C;}$  typical values.  
 (2)  $T_j = 125 \text{ }^\circ\text{C;}$  maximum values.  
 (3)  $T_j = 25 \text{ }^\circ\text{C;}$  maximum values.

**Fig 9. On-state current characteristics**



$R_{GK} = 1 \text{ k}\Omega.$

**Fig 10. Normalized latching current as a function of junction temperature**



## 7. Package information

Epoxy meets requirements of UL94 V-0 at 1/8 inch.

8. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

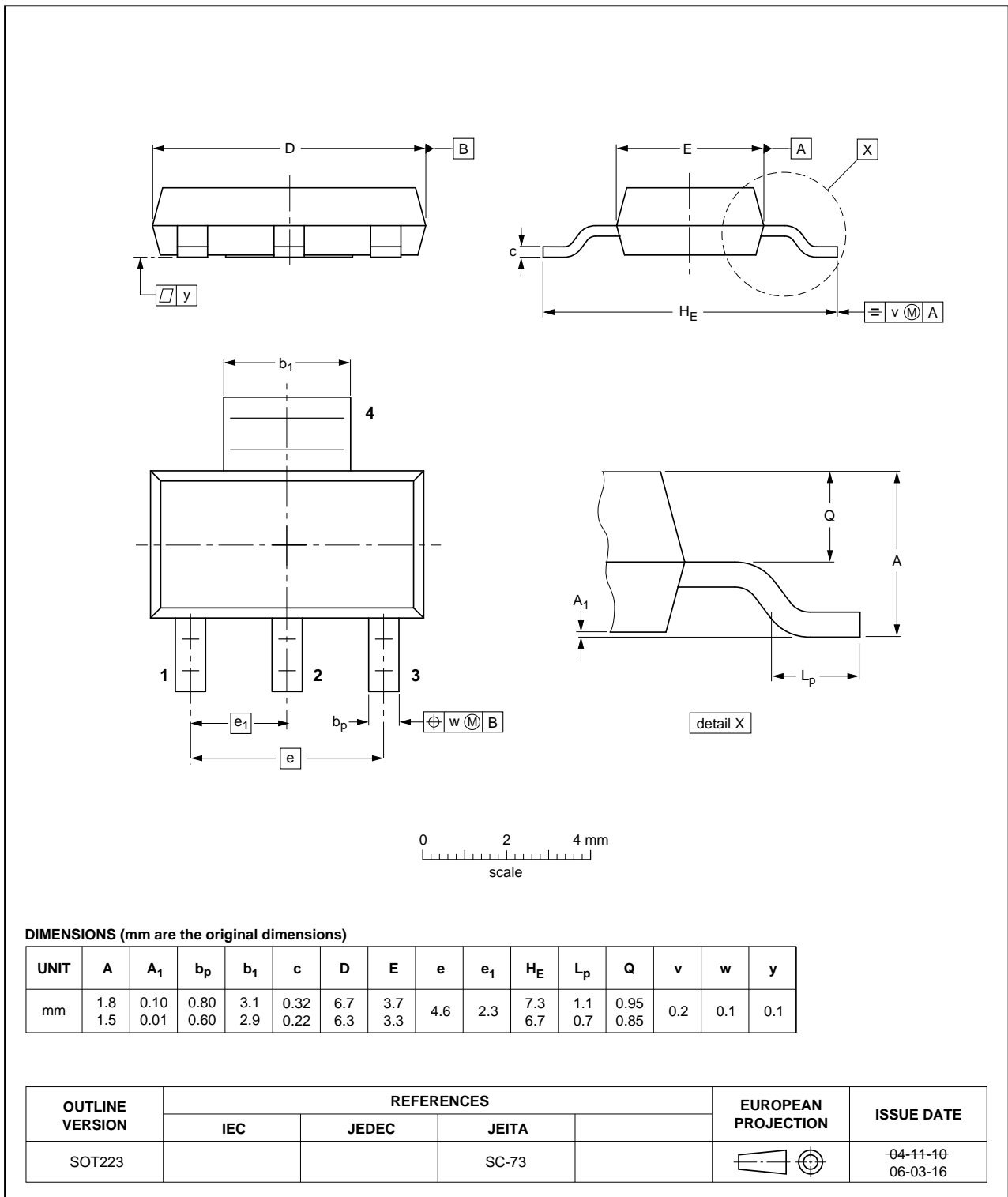
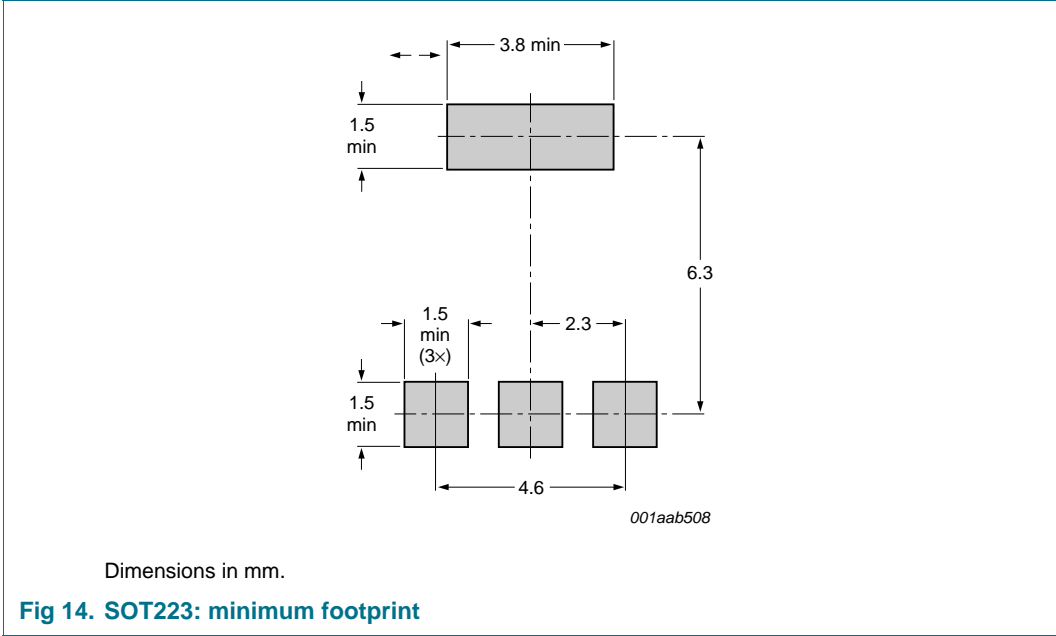


Fig 13. Package outline SOT223 (SC-73)



9. Mounting

9.1 Mounting instructions



## 10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MCR08BT1 v.4	20111102	Product data sheet		MCR08BT1 v.3
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>		
MCR08BT1 v.3	20041129	Product data sheet		MCR08BT1_HG v.2
MCR08BT1_HG v.2	20011023	Product specification		MCR08BT1 v.1
MCR08BT1 v.1	20010701	Product specification		-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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